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**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (canceled) An apparatus comprising:

a control circuit to generate a channel enable signal based on control information from a processor at a first clock signal having a first clock frequency, the channel enable signal selecting a channel for a satellite in a global positioning system (GPS), the channel operating at a coarse/acquisition (C/A) clock signal having a second clock frequency;

an increment register to store an increment value for the selected channel at the first clock signal; and

an accumulator coupled to the increment register and the control circuit to generate a PN clock signal using the increment value.

2. (canceled) The apparatus of claim 1 wherein the control information includes at least one of channel select information, an initial count, the increment value, and PN command.

3. (currently amended) An ~~The~~ apparatus ~~of claim 2~~ comprising:

a control circuit to generate a channel enable signal based on control information from a processor at a first clock signal having a first clock frequency, the channel enable signal selecting a channel for a satellite in a global positioning system (GPS), the channel operating at a coarse/acquisition (C/A) clock signal having a second clock frequency, the control information including at least one of channel select information, an initial count, an increment value, and PN command;

an increment register to store the increment value for the selected channel at the first clock signal; and

an accumulator coupled to the increment register and the control circuit to generate a PN clock signal using the increment value;

wherein the control circuit comprises:

a decoder to decode the channel select information, the decoded channel select information providing the channel enable signal;

a channel enable register coupled to the decoder to store the channel enable signal at the first clock signal;

a counter coupled to the channel enable register to update a count from the initial count at the first clock signal, the counter generating a terminal signal when the count reaches a terminal count; and

a logic circuit coupled to the counter and the channel enable register to generate a load signal from the PN command to load the initial count to the counter and a reset signal from the terminal signal to reset the channel enable register.

4. (currently amended) The apparatus of claim 3 [[2]] wherein the accumulator comprises:

an accumulating register to store a numerically controlled oscillator (NCO) value at a current cycle of the first clock signal, the NCO value providing the PN clock; and

an adder coupled to the accumulating register and the increment register to generate a sum of the increment value and the NCO value using a shift command from the PN command, the sum being loaded into the accumulating register and corresponding to the NCO value at a next cycle of the first clock signal.

5. (original) The apparatus of claim 4 wherein the adder shifts the increment value in a direction according to the shift command.

6. (original) The apparatus of claim 5 wherein the adder shifts the increment value one bit to the left if the shift command is a left shift command.

7. (original) The apparatus of claim 5 wherein the adder shifts the increment value one bit to the right if the shift command is a right shift command.

8. (original) The apparatus of claim 4 wherein a most significant bit (MSB) of the NCO value provides the PN clock to the PN generator.

9. (currently amended) The apparatus of claim 3 [[1]] wherein the first and second clock frequencies are approximately 8.184 MHz and 1.023 MHz, respectively.

10. (currently amended) The apparatus of claim 3 [[1]] wherein the channel enable signal is one of twelve enable signals corresponding to twelve satellites in the GPS.

11. (canceled) A method comprising:

generating a channel enable signal based on control information from a processor at a first clock signal having a first clock frequency, the channel enable signal selecting a channel for a satellite in a global positioning system (GPS), the channel operating at a coarse/acquisition (C/A) clock signal having a second clock frequency;

storing an increment value for the selected channel at the first clock signal; and

generating a pseudo-random noise (PN) clock signal to a PN generator using the increment value.

12. (canceled) The method of claim 11 wherein the control information includes at least one of channel select information, an initial count, the increment value, and PN command.

13. (original) A ~~The~~ method ~~of claim 12~~ comprising:

generating a channel enable signal based on control information from a processor at a first clock signal having a first clock frequency, the channel enable signal selecting a channel for a satellite in a global positioning system (GPS), the channel operating at a coarse/acquisition (C/A) clock signal having a second clock frequency, the control information including at least one of channel select information, an initial count, an increment value, and PN command;

storing the increment value for the selected channel at the first clock signal; and

generating a pseudo-random noise (PN) clock signal to a PN generator using the increment value;

wherein generating the channel enable signal comprises:

decoding the channel select information, the decoded channel select information providing the channel enable signal;

storing the channel enable signal at the first clock signal;

updating a count from the initial count at the first clock signal to generate a terminal signal when the count reaches a terminal count; and

generating a load signal from the PN command to load the initial count to the counter and a reset signal from the terminal signal to reset the channel enable register.

14. (currently amended) The method of claim 13 [[12]] wherein generating the PN clock comprises:

storing a numerically controlled oscillator (NCO) value at a current cycle of the first clock signal in an accumulating register, the NCO value providing the PN clock; and

generating a sum of the increment value and the NCO value using a shift command from the PN command, the sum being loaded into the accumulating register and corresponding to the NCO value at a next cycle of the first clock signal.

15. (original) The method of claim 14 wherein generating the sum comprises shifting the increment value in a direction according to the shift command.

16. (original) The method of claim 15 wherein shifting the increment value comprises shifting the increment value one bit to the left if the shift command is a left shift command.

17. (original) The method of claim 15 wherein shifting the increment value comprises shifting the increment value one bit to the right if the shift command is a right shift command.

18. (original) The method of claim 14 wherein a most significant bit (MSB) of the NCO value provides the PN clock to the PN generator.

19. (currently amended) The method of claim 13 [[11]] wherein the first and second clock frequencies are approximately 8.184 MHz and 1.023 MHz, respectively.

20. (currently amended) The method of claim 13 [[11]] wherein the channel enable signal is one of twelve enable signals corresponding to twelve satellites in the GPS.

21. (canceled) A receiver comprising:

a processor to generate control information;

a pseudo-random noise (PN) code generator to generate a PN sequence at a PN clock signal to a correlator of a global positioning system (GPS) base-band system; and

a code numerically controlled oscillator (NCO) coupled to the PN code generator and the processor to generate the PN clock signal based on the control information, the code NCO comprising:

a control circuit to generate a channel enable signal based on the control information at a first clock signal having a first clock frequency, the channel enable signal selecting a channel for a satellite in a global positioning system (GPS), the channel operating at a coarse/acquisition (C/A) clock signal having a second clock frequency,

an increment register to store an increment value for the selected channel at the first clock signal, and

an accumulator coupled to the increment register and the control circuit to generate the PN clock signal using the increment value.

22. (canceled) The receiver of claim 21 wherein the control information includes at least one of channel select information, an initial count, the increment value, and PN command.

23. (currently amended) A ~~The~~ receiver ~~of claim 22~~ comprising:

a processor to generate control information including at least one of channel select information, an initial count, an increment value, and PN command;

a pseudo-random noise (PN) code generator to generate a PN sequence at a PN clock signal to a correlator of a global positioning system (GPS) base-band system; and

a code numerically controlled oscillator (NCO) coupled to the PN code generator and the processor to generate the PN clock signal based on the control information, the code NCO comprising:

a control circuit to generate a channel enable signal based on the control information at a first clock signal having a first clock frequency, the channel enable signal selecting a channel for a satellite in a global positioning system (GPS), the channel operating at a coarse/acquisition (C/A) clock signal having a second clock frequency,

an increment register to store the increment value for the selected channel at the first clock signal, and

an accumulator coupled to the increment register and the control circuit to generate the PN clock signal using the increment value;

wherein the control circuit comprises:

a decoder to decode the channel select information, the decoded channel select information providing the channel enable signal;

a channel enable register coupled to the decoder to store the channel enable signal at the first clock signal;

a counter coupled to the channel enable register to update a count from the initial count at the first clock signal, the counter generating a terminal signal when the count reaches a terminal count; and

a logic circuit coupled to the counter and the channel enable register to generate a load signal from the PN command to load the initial count to the counter and a reset signal from the terminal signal to reset the channel enable register.

24. (currently amended) The receiver of claim 23 [[22]] wherein the accumulator comprises:

an accumulating register to store a numerically controlled oscillator (NCO) value at a current cycle of the first clock signal, the NCO value providing the PN clock; and

an adder coupled to the accumulating register and the increment register to generate a sum of the increment value and the NCO value using a shift command from the PN command,

the sum being loaded into the accumulating register and corresponding to the NCO value at a next cycle of the first clock signal.

25. (original) The receiver of claim 24 wherein the adder shifts the increment value in a direction according to the shift command.

26. (original) The receiver of claim 25 wherein the adder shifts the increment value one bit to the left if the shift command is a left shift command.

27. (original) The receiver of claim 25 wherein the adder shifts the increment value one bit to the right if the shift command is a right shift command.

28. (original) The receiver of claim 24 wherein a most significant bit (MSB) of the NCO value provides the PN clock to the PN generator.

29. (currently amended) The receiver of claim 23 [[21]] wherein the first and second clock frequencies are approximately 8.184 MHz and 1.023 MHz, respectively.

30. (currently amended) The receiver of claim 23 [[21]] wherein the channel enable signal is one of twelve enable signals corresponding to twelve satellites in the GPS.